



Fig. 2

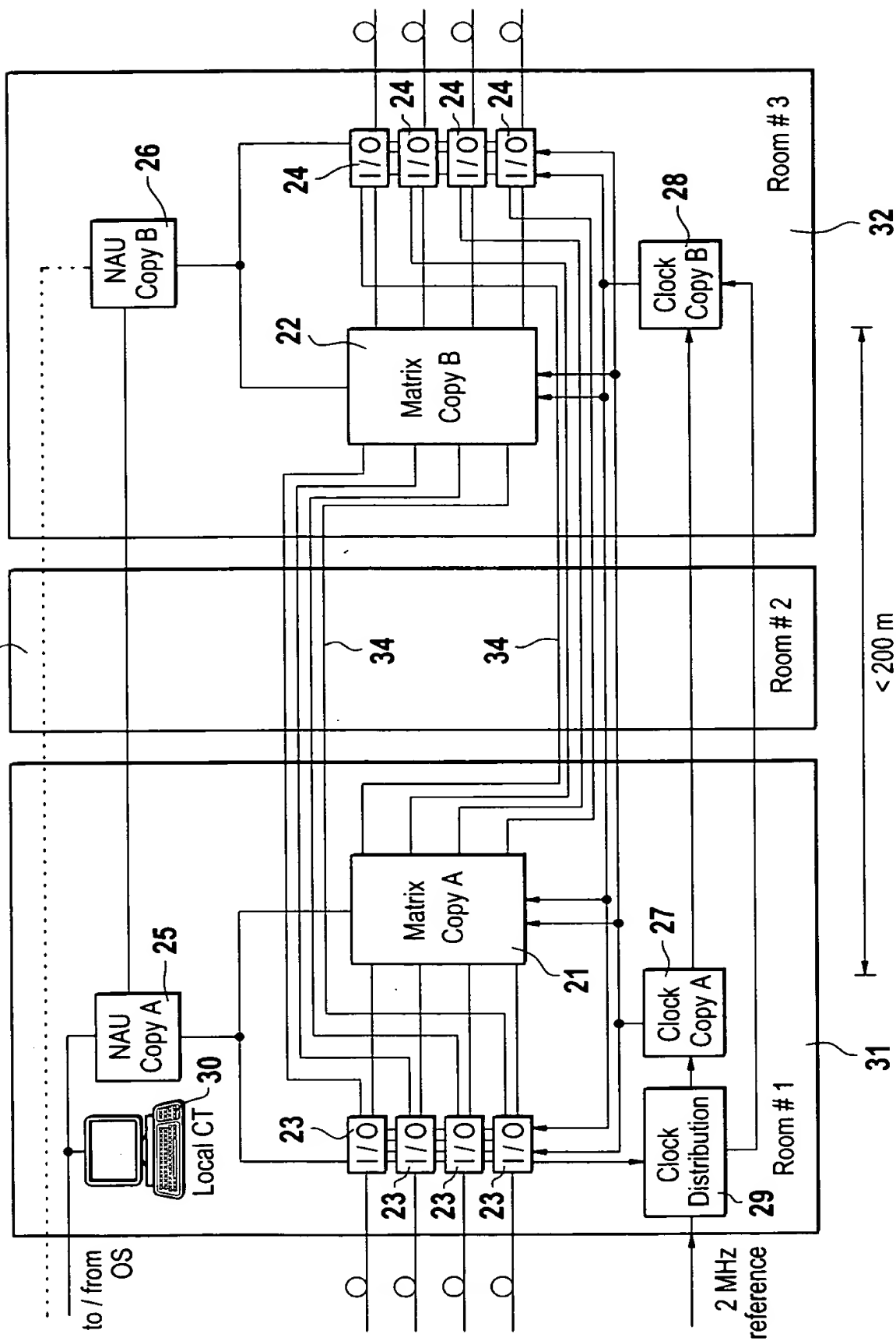


Fig. 3

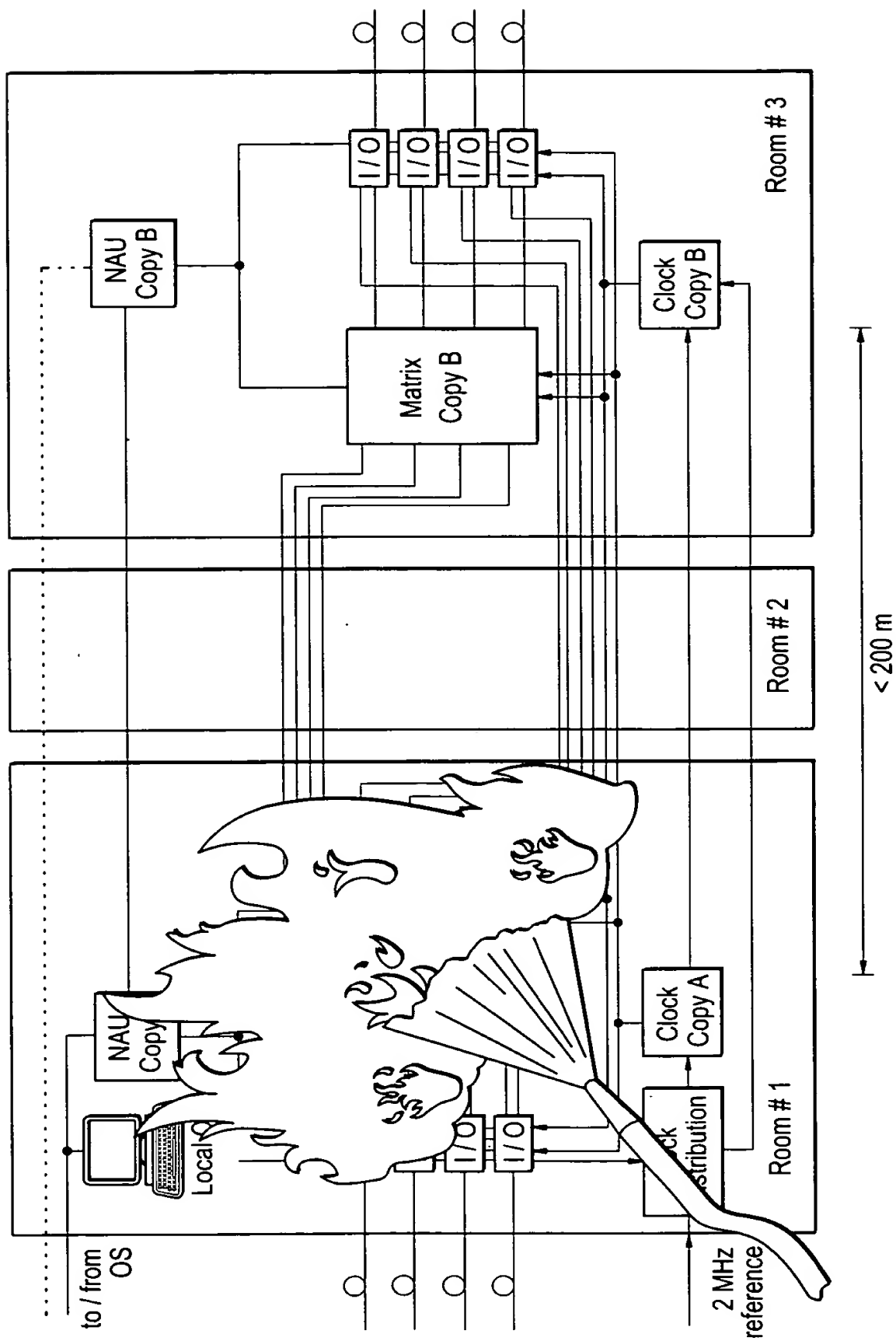


Fig. 4

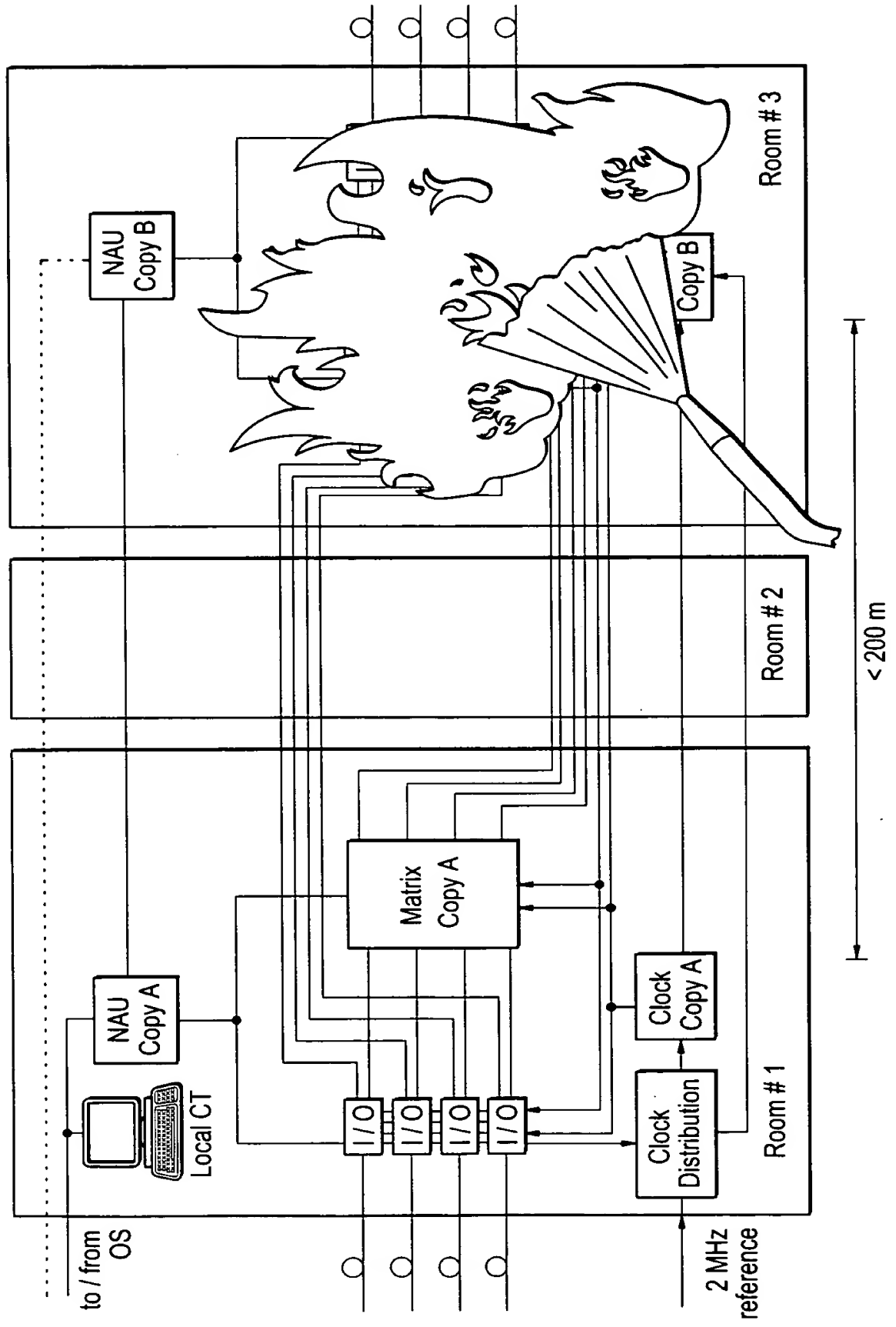


Figure 5 shows a schematic diagram of a system architecture. The diagram is divided into three main sections: Room #1, Room #2, and Room #3. Room #1 contains a 'Local CT' (Control Terminal) connected to 'NAU Copy A' and 'Matrix Copy A'. It also features a 'Clock Distribution' block and a 'Clock Copy A' block. Room #2 contains a large starburst symbol representing a fault or event. Room #3 contains 'NAU Copy B', 'Matrix Copy B', and 'Clock Copy B'. Each room has four 'I/O' blocks. A '2 MHz reference' signal is input to Room #1. A distance of '< 200 m' is indicated between Room #1 and Room #3. A 'to / from OS' connection is shown at the top left.

Fig. 5

